WHAT IS CLAIMED IS:

1. A semiconductor chip having a substrate of a first conductivity type, the chip comprising:

a pad;

an electrostatic discharge (ESD) positive ring;

an ESD negative ring; and

a plurality of floating lateral clamp diodes connected to the pad so that a first floating lateral clamp diode is connected to the pad and the positive ring, and a second floating lateral clamp diode is connected to the pad and the negative ring.

2. The chip of claim 1 wherein a floating lateral clamp diode comprises:

a well of a second conductivity type formed in the substrate, the well having a surface and a dopant concentration; and

a plurality of spaced-apart first regions of the first conductivity type, each first region having a surface, the plurality of first regions being electrically connected together, and formed in the well so that the surface of the well encircles the surface of each first region.

3. The chip of claim 2 and further comprising ~~a second region of the second conductivity type, the~~

second region having a surface, and being formed in the well so that the surface of the second region encircles the surface of the well that encircles the surface of each first region, the second region having a dopant concentration that is greater than the dopant concentration of the well.

4. The chip of claim 1 wherein the ESD positive ring encircles the periphery of the chip.

5. The chip of claim 1 wherein the ESD negative ring encircles the periphery of the chip.

6. The chip of claim 1 and further including an ESD switch connected to the ESD positive ring and the ESD negative ring.

7. The chip of claim 1 and further including a plurality of ESD switches which are each connected to the ESD positive ring and the ESD negative ring.

8. The chip of claim 7 wherein an ESD switch is located in a corner of the chip.

9. The chip of claim 7 wherein one or more ESD switches are located between two adjacent corners of the chip.

10. The chip of claim 1 wherein a floating lateral clamp diode comprises:

a well of a second conductivity type formed in the substrate, the well having a surface and a dopant concentration; and

a first region of the second conductivity type formed in the well, the first region having a surface, and a dopant concentration that is greater than the dopant concentration of the well;

a plurality of spaced-apart second regions of the first conductivity type, each second region having a surface, the plurality of second regions being electrically connected together, and formed in the first region so that the surface of the first region encircles the surface of each second region.

11. The chip of claim 10 and further comprising a third region of the second conductivity type, the third region having a surface, and being formed in the first region so that the surface of the third region encircles the surface of the first region that encircles the surface of each second region, the third region having a dopant concentration that is greater than the dopant concentration of the well.

12. The chip of claim 1 wherein the ESD positive ring and the ESD negative ring are floating.

13. The chip of claim 1 wherein the ESD positive ring is connected to one or more VCC package pins.

14. The chip of claim 1 wherein the ESD negative ring is connected to one or more ground package pins.

15. A semiconductor chip having a substrate of a first conductivity type, the chip comprising:

a plurality of pads;

an electrostatic discharge (ESD) negative ring;

a plurality of ESD positive lines;

a plurality of ESD switches connected to the ESD positive lines and the ESD negative ring so that each positive line is connected to the negative ring via an ESD switch;

a plurality of first floating lateral clamp diodes connected to the pads so that each first floating lateral clamp diode is connected to a pad and the negative ring; and

a plurality of second floating lateral clamp diodes connected to the pads so that each second floating lateral clamp diode is connected to a pad ~~and a positive line.~~

16. The chip of claim 15 wherein a plurality of second floating lateral clamp diodes are connected to ~~a positive line.~~

17. The chip of claim 15 wherein a first floating lateral clamp diode comprises:

a well of a second conductivity type formed in the substrate, the well having a surface and a dopant concentration; and

a plurality of spaced-apart first regions of the first conductivity type, each first region having a surface, the plurality of first regions being electrically connected together, and formed in the well so that the surface of the well encircles the surface of each first region.

18. The chip of claim 17 and further comprising a second region of the second conductivity type, the second region having a surface, and being formed in the well so that the surface of the second region encircles the surface of the well that encircles the surface of each first region, the second region having a dopant concentration that is greater than ~~the dopant concentration of the well~~.

19. The chip of claim 15 wherein the ESD negative ring encircles the periphery of the chip.

20. The chip of claim 15 wherein a first floating lateral clamp diode comprises:

a well of a second conductivity type formed in the substrate, the well having a surface and a dopant concentration; and

a first region of the second conductivity type formed in the well, the first region having a surface, and a dopant concentration that is greater than the dopant concentration of the well;

a plurality of spaced-apart second regions of the first conductivity type, each second region having a surface, the plurality of second regions being electrically connected together, and formed in the first region so that the surface of the first region encircles the surface of each second region.

21. The chip of claim 20 and further comprising a third region of the second conductivity type, the third region having a surface, and being formed in the first region so that the surface of the third region encircles the surface of the first region that encircles the surface of each second region, the third region having a dopant concentration that is greater than the dopant concentration of the well.

22. The chip of claim 15 wherein an ESD positive line is connected to one or more VCC package pins.

23. The chip of claim 15 wherein the ESD negative ring is connected to one or more ground package pins.

24. A method for forming a semiconductor chip having a substrate of a first conductivity type, the method comprising the steps of:

forming a pad;

forming an electrostatic discharge (ESD) positive ring;

forming an ESD negative ring; and

forming a plurality of floating lateral clamp diodes connected to the pad so that a first floating lateral clamp diode is connected to the pad and the positive ring, and a second floating lateral clamp diode is connected to the pad and the negative ring.

25. The method of claim 24 wherein the step of forming a floating lateral clamp diode comprises the steps of:

forming a well of a second conductivity type in the substrate, the well having a surface and a dopant concentration; and

forming a plurality of spaced-apart first regions of the first conductivity type in the well, each first region having a surface, the plurality of first regions being electrically connected together, and formed in the well so that the surface of the well encircles the surface of each first region.

26. The method of claim 25 and further comprising the step of forming a second region of the second conductivity type in the well, the second region having a surface, and being formed in the well so that the surface of the second region encircles the surface of the well that encircles the surface of each first region, the second region having a dopant concentration that is greater than the dopant concentration of the well.

27. A method for forming a semiconductor chip having a substrate of a first conductivity type, the method comprising the steps of:

forming a plurality of pads;

forming an electrostatic discharge (ESD) negative ring;

forming a plurality of ESD positive lines;

forming a plurality of ESD switches connected to the ESD positive lines and the ESD negative ring so

that each positive line is connected to the negative ring via an ESD switch;

forming a plurality of first floating lateral clamp diodes connected to the pads so that each first floating lateral clamp diode is connected to a pad and the negative ring; and

forming a plurality of second floating lateral clamp diodes connected to the pads so that each second floating lateral clamp diode is connected to a pad and a positive line.

28. The method of claim 27 wherein a plurality of second floating lateral clamp diodes are connected to a positive line.

29. The method of claim 27 wherein the step of forming a first floating lateral clamp diode comprises the steps of:

forming a well of a second conductivity type in the substrate, the well having a surface and a dopant concentration; and

forming a plurality of spaced-apart first regions of the first conductivity type in the well, each first region having a surface, the plurality of first regions being electrically connected together, and formed in the well so that the surface of the well encircles the surface of each first region.

30. The method of claim 29 and further comprising the step of forming a second region of the second conductivity type in the well, the second region having a surface, and being formed in the well so that the surface of the second region encircles the surface of the well that encircles the surface of each first region, the second region having a dopant concentration that is greater than the dopant ~~concentration of the well.~~

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